



PRODUCT OUTLINE

CM2311de – SAR ADC/DAC Subsystem
11-bit, 1–5MSPS, Hybrid SAR

Part Number

■ CM2311de

Features

- 11-bit/3.7MSPS SAR ADC
- Unbuffered output, 11-bit/10.4MSPS DAC
- Independent high and low reference inputs
- Digital parallel input, digital serial output
- End of conversion indicator
- No missing code
- Indicative area: 0.165mm²

Applications

- Smart Grid
- Instrumentation
- Monitoring applications
- Consumer electronics

Technology

- AMS 0.35µm B3C3/B4C3 CMOS

Deliverables

- Datasheet/Integration Guide
- HDL Model
- Flat GDSII database/LVS netlist
- Customer Support

Status

- GDS Available

Overview

This macro-cell is a general purpose, Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) subsystem. The DAC employs a hybrid architecture, using 6-bit resistive and 5-bit capacitive sub-DACs.

It is a standard part, enabling multiple system utilizations. The core operates in 11-bit linear mode and uses one 3.3V analog and one 3.3V digital supplies.

The core includes built-in sample-and-hold functionality.

Functional Diagram

