# PHY_LPDDR4/4x/5/5x

## Overview

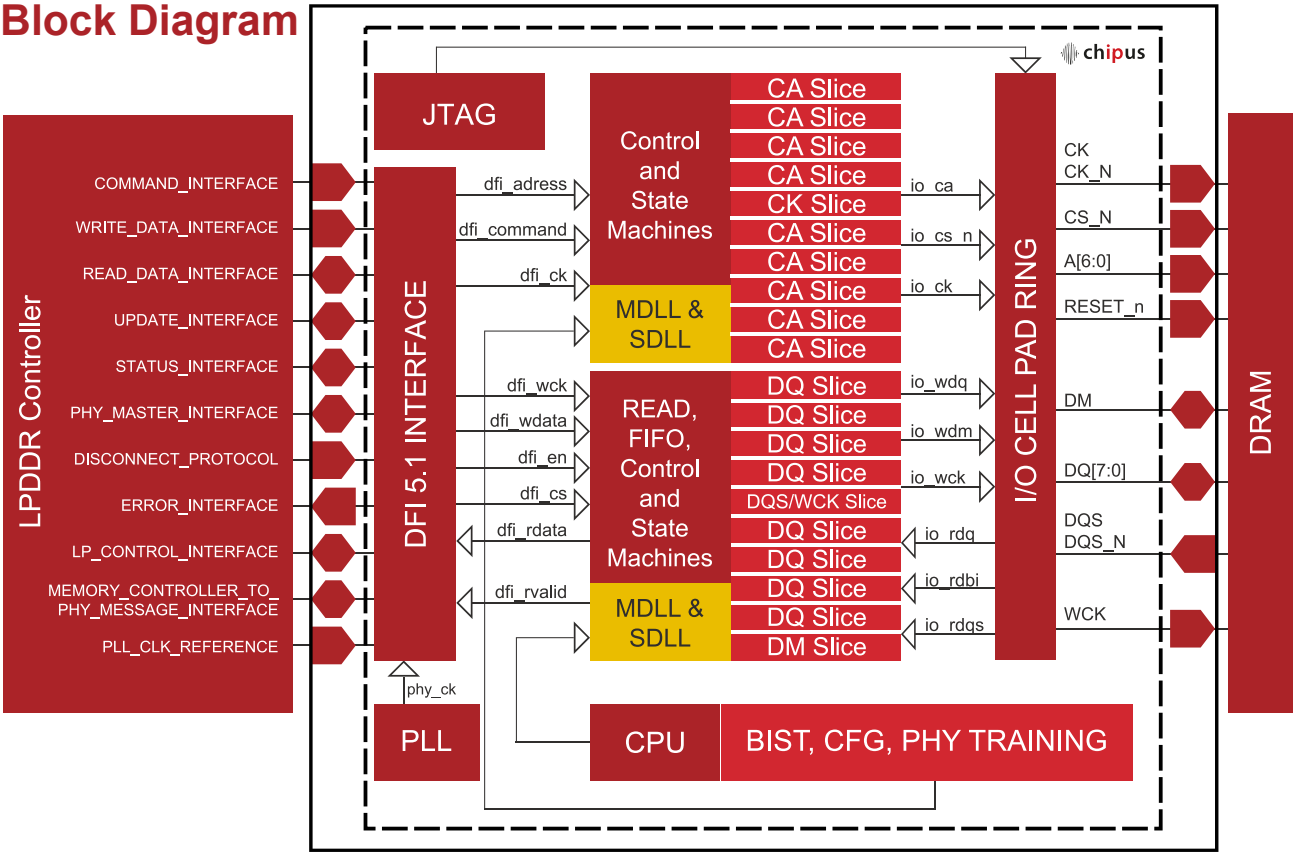
The Chipus LPDDR PHY is designed to support LPDDR4, LPDDR4x, LPDDR5 and LPDDR5x SDRAM.

This allows the host SoC to easily be configured for the specific DDR SDRAM variant used in the system via simple software control allowing one chip to target multiple applications using different DDR types.

The Chipus DDR PHY has been optimized to take advantage of the memory configurations and packaging to reduce the total memory subsystem power and area.

The DDR PHY is designed to comply with DFI 5.1 memory standard so the PHY can work seamlessly with DDR Memory controllers from any supplier that compliant with the DFI 5.1 Standard.

## Block Diagram




## Highlights

- Supports JEDEC SDRAM standards including LPDDR4 (1.1V), LPDDR4x (0.6V), LPDDR5/5x (0.5V)
- Supports data rates up to 4,266 Mbps LPDDR4/LPDDR5 and up to 8,533 Mbps LPDDR5x
- Support for 16, 32 and 64-bit operation
- GDSII-based “hard” PHY avoids timing closure problems common with “soft” RTL-based DDR PHYs
- Designed for rapid integration with DFI 5.1 compliant memory controller
- Includes application specific, multi-protocol DDR I/Os including programmable drive strength and ODT
- DFI 5.1 compliant controller interface
- Low Power Mode Support
- DATA Retention
- Scan and JTAG Testing
- At speed internal and external BIST testing for Chip Probe and Package ATE testing
- PHY Independent Training and Calibration

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## Deliverables

- Databook
- User Guide
- Behavioral RTL model
- LEF file
- .LIB file
- GDSII Layout Database
- CDL
- SCAN and JTAG Vectors
- IBIS Models for PCB Design and verification

## Target Applications

- LPDDR4/4x - 4,266 Mbps
- LPDDR5 - 6,400 Mbps
- LPDDR5x - 8,533 Mbps

## Key Features

- Operating range 533 – 8,533 Mbps LPDDR4/LPDDR4x/LPDDR5/LPDDR5x mode
- DFI 1:2 and DFI 1:4 clocking support
  - 1:2 DFI_CLK = 1,066 MHz
  - LPDDR4/4x/5/5x – 4,266 Mbps
  - 1:4 DFI_CLK = 533 MHz
  - LPDDR4/4x/5/5x – 4,266 Mbps
  - 1:4 DFI_CLK = 800 MHz
  - LPDDR5 – 6,400 Mbps
  - 1:4 DFI_CLK = 1,066 MHz
  - LPDDR5 – 8,533 Mbps
- PHY includes PVT compensated I/Os that are compatible with wire bond and flip chip (ESD included)
- Small PHY area – (tbd)mm2
- Low power – (tbd)/(tbd)/(tbd) mW (READ, WRITE, and IDLE)
- Configurable external memory channel widths in 16-bit, 32-bit and 64-bit
- Programmable I/O output drive strength and On Die Termination (ODT) impedance with dynamic PVT compensation
- Support for Per Bit Deskew
- At speed Internal and External Loopback BIST testing in PHY Standalone mode for Chip Probe Testing on DQ/DQS
- Scan and JTAG/BSR standard testing
- AHB Register interface for easy PHY configuration and control for non-DFI related features
- Low power stand by using DFI Compliant LP interface
- DATA Retention
- PHY Independent DDR Training, Dynamic training and DDR Initialization Support using embedded memory controller and 32-bit processor
  - CA Training
  - Write Leveling
  - Read Gate Training
  - Read EYE training EYE Scan and Bit Deskew
  - READ EYE DFE
  - Write EYE Training EYE Scan and Bit Deskew
  - WRITE EYE DFE
  - CK and WCK Duty Cycle Training
  - READ DQS Duty Cycle Training
  - READ and WRITE OSC Training
  - READ and WRITE Offset Calibration
  - READ and WRITE PreEmphasis Calibration


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